

Hall Ticket Number:

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Code No. : 13466 N/O

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD*Accredited by NAAC with A++ Grade***B.E. (E.C.E.) III-Semester Main & Backlog Examinations, Jan./Feb.-2024****Digital Logic Design**

Time: 3 hours

Max. Marks: 60

*Note: Answer all questions from Part-A and any FIVE from Part-B***Part-A (10× 2 = 20 Marks)**

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	State and prove De Morgan's theorem.	2	1	1	1	1
2.	Realize 2-input EX-OR gate using NOR gate.	2	1	1	2	1
3.	Compare the function of decoder and demultiplexer?	2	1	2	1	1
4.	Design half adder using only NAND gates?	2	2	2	2	1
5.	Implement the following boolean expressions using a suitable PLA. $A(x,y,z) = \sum m(1,2,4,6)$ $B(x,y,z) = \sum m(0,1,6,7)$	2	3	3	3	1
6.	What are the steps involved in state minimization?	2	1	3	1	1
7.	What is the difference between \$display and \$monitor?	2	1	4	1	1
8.	Write the verilog program for 2 bit comparator in gate level modeling?	2	3	4	2	1
9.	What is the significance of sequential and parallel blocks?	2	1	5	1	1
10.	Distinguish Melay and Moore FSM?	2	2	5	2	1
Part-B (5×8 = 40 Marks)						
11. a)	How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property?	4	2	1	2	1
b)	Simplify the following function using K-map and implements it using basic logic gates. $F(a,b,c,d) = \sum m(0,2,8,9,10,14) + d(3,7,11,15)$	4	3	1	3	1
12. a)	Design and explain a 4-bit carry look ahead adder.	4	2	2	3	1
b)	Outline full adder and also implement it using 4X1 multiplexer.	4	2	2	3	1
13. a)	Design a 4-Bit bidirectional shift register using JK flip-flops having right and left data inputs and mode control M such that M=0 left shift, M=1 right shift.	4	3	3	4	1
b)	Design a sequence detector which produces an output '1' every time the sequence '1001' is detected and an output '0' at all other times. Consider non overlapping sequence.	4	4	3	3	1

Contd... 2

14. a)	Discuss various gate delays in verilog HDL?	3	2	4	2	1
b)	Develop a verilog code for the following function. $F(A,B,C,D) = \sum m((0,3,4,5,11,12,13,15)+d(2,6,8))$ in gate level model and write test bench to verify its functionality?	5	4	4	3	1
15. a)	Draw and explain the logic synthesis flow chart.	4	2	5	2	1
b)	Explain different types of conditional statements used in behavioral modeling.	4	3	5	2	1
16. a)	Write short notes on binary codes	4	1	1	2	1
b)	What is encoder? Design an octal to binary encoder.	4	3	2	3	1
17.	Answer any <i>two</i> of the following:					
a)	Design 4 bit synchronous up counter using D-flip flop.	4	3	3	4	1
b)	Write a verilog code using switch level modeling for universal gates?	4	2	4	3	1
c)	Write a verilog code for 8:1 MUX using behavioral modeling?	4	2	5	3	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	38.75%
iii)	Blooms Taxonomy Level – 3 & 4	41.25%
